

# SPECIFICATION

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## ***WAFER INCLUDING AN In-CONTAINING-COMPOUND SEMICONDUCTOR SURFACE LAYER, AND METHOD FOR PROFILING ITS CARRIER CONCENTRATION***

### Background of Invention

[0001] Field of the Invention

[0002] The present invention relates to compound semiconductor wafers, and in particular to the profiling of carrier concentration in In-containing compound semiconductor wafers.

[0003] Description of the Background Art

[0004] Well-known methods of profiling carrier concentration within semiconductor wafers may be grossly divided into methods that measure Hall coefficient, and the  $C/V$  technique, which measures capacitance/voltage characteristics.

[0005] With the Hall-coefficient measuring methods, the carrier concentration of the semiconductor wafer cannot be measured nondestructively since a rectangular test piece for measuring must be cut out of a semiconductor wafer. This means that the carrier concentration of wafers themselves into which semiconductor devices are built cannot be profiled. Likewise, the Hall coefficient pertains to the test piece as a whole, and does not allow profiling of carrier concentration locally within the test piece.

[0006] In terms of the  $C/V$  technique, ordinarily a Schottky diode that is metal vapor-

deposited onto the semiconductor wafer is formed, and an ac voltage of minute amplitude is superimposed onto a dc reverse-bias voltage to measure the  $C/V$  characteristics. Being that the region within the semiconductor wafer on which the Schottky diode for measuring  $C/V$  characteristics is formed cannot thereafter be employed for semiconductor device formation, the routine  $C/V$  technique cannot be said to be a non-invasive profiling method.

[0007] Likewise, with regard to compound semiconductor wafers, the routine  $C/V$  technique is not a very attractive method. The reason why is that in respect of compound semiconductor wafers, the barrier height of Schottky diodes is low, oxide-film formation cannot be controlled, and further, problems such as chemical reactions between metals and the compound semiconductor can arise.

[0008] Therein, to profile carrier concentration in a compound semiconductor wafer, electrochemical  $C/V$  techniques utilizing an electrolyte as an electrode have been used. (See for example, *J. Electrochem. Soc.*, Vol. 133, 1986, pp. 2278-2283.)

[0009] Reference is made to Fig. 2, a block diagram schematically illustrating a conventional electrochemical  $C/V$  technique. In the electrochemical  $C/V$  analyzer set out in Fig. 2, the interior of a cell 1 is filled with an electrolyte 2 such as an aqueous HCl solution. A calomel electrode 3 as a reference electrode is inserted into the cell 1. The cell 1 has a ring-shaped opening 1a, and a compound semiconductor wafer 4 whose  $C/V$  characteristics are to be measured is contacted with the electrolyte 2 via the opening 1a, wherein the electrolyte 2 acts as one of the electrodes. A probe electrode 5 as the other electrode is contacted on the compound semiconductor wafer 4. An electrical analyzing unit 6 supplies a dc reverse-bias voltage and around a 3000-Hz ac superimposed voltage to the reference electrode 3 and the probe electrode 5 to measure the  $C/V$  characteristics.

[0010] In a depth  $w$  from the surface where the compound semiconductor wafer 4 is in contact with the electrolyte electrode 2, the carrier concentration  $N(\text{cm}^{-3})$  within the wafer may be determined using the following formula (1).

$$[0011] \quad N(w) = (-C^3 / q \epsilon A^2) (dC/dV)^{-1} \quad (1)$$

[0012] Herein,  $w$  expresses the depth from the wafer surface to the edge of the depletion

layer. That is,  $N(w)$  expresses the carrier concentration  $N$  in the depth  $w$  from the wafer surface. Likewise,  $C$  expresses capacitance measured by a dc reverse-bias voltage;  $q$ , electronic charge;  $\epsilon$ , permittivity;  $A$ , measurement area; and  $dC$ , variation in capacitance depending on variation  $dV$  in the superimposed ac voltage. Here, the depth  $w$  may be found from the following formula (2).

$$[0013] \quad w = \epsilon A / C \quad (2)$$

[0014] In terms of an electrochemical  $C/V$  technique utilizing an electrolyte electrode as described above, profiling carrier concentration through depths of more than  $3 \mu\text{m}$  is difficult unless a reverse-bias voltage that exceeds 10 V is applied. However, wherein an electrolyte electrode such as, e.g., an aqueous HCl solution is utilized, electrical breakdown of the electrolyte sets in when a high reverse-bias voltage in excess of 10 V is applied, giving rise to problems in that bubbles of hydrogen and oxygen cling to the wafer surface and make it impossible to measure the  $C/V$  characteristics. Applying too high a voltage can also give rise to problems in that the leakage current grows large, and electrolyte leakage occurs.

[0015] Consequently, in conventional electrochemical  $C/V$  analyzers, the maximum value of the reverse-bias applied voltage is in general limited to 10 V. To work around this limitation, carrier concentration through depths of more than  $3 \mu\text{m}$  is profiled by repeating  $C/V$  analysis using an applied voltage of under 10 V, and wafer surface etching using a photo-etching process.

[0016] This means that, as shown in Fig. 2, the cell 1 in a conventional electrochemical  $C/V$  analyzer is furnished with a light-receiving window 1b. By shining light 7 onto the wafer surface where it contacts the electrolyte 2 at the ring-shaped opening 1a, the electrolyte 2 works as an etchant and the wafer surface is removed to a predetermined depth by photo-etching. Then a succeeding  $C/V$  analysis is performed with the surface freshly formed by the etching as a new reference.

[0017] With this method of profiling carrier concentration by repeating  $C/V$  analysis and photo-etching in this way, time is required for the etching; for a  $C/V$  analysis in order to profile carrier-concentration/distribution about  $2 \mu\text{m}$  in the depth direction, around 1 hour is necessary. Furthermore, being that the photo-etched region cannot

thereafter be employed for semiconductor device formation, the conventional electrochemical  $C/V$  technique cannot be said to be a non-invasive profiling method.

[0018] Moreover, In-containing compound semiconductor wafers for forming optical-communications photo detectors must be furnished with an epitaxial layer 5 to 8  $\mu\text{m}$  in thickness, and if the carrier concentration within an epitaxial layer that thick is profiled by the repeating of  $C/V$  analysis and photo-etching processes, the  $C/V$  analysis alone ends up taking around 3 to 4 hours. Still further, performing photo-etching with consistency is not easy, and gaining high precision in  $C/V$  analysis is difficult.

## Summary of Invention

[0019] Taking the above-described issues in the prior art into consideration, an object of the present invention is to develop a method of non-invasively profiling carrier concentration/distribution in a short time to a depth of several  $\mu\text{m}$  within an In-containing compound semiconductor wafer, and at the same time to provide the profiled wafer itself for use directly in device fabrication.

[0020] A method as defined by one mode of the present invention, which employing the  $C/V$  technique profiles carrier concentration in a wafer including an In-containing-compound semiconductor surface layer, is characterized in non-invasively profiling carrier concentration by contacting a liquid electrode on the wafer surface, and without using a photo etching process, employing an applied voltage that is up to a voltage surpassing 10V.

[0021] Here, an aqueous EDTA solution is preferably utilized as the liquid electrode. Likewise, the aqueous EDTA solution preferably contains 80% or more EDTA. Furthermore, liquid iron or a metal gallium (Ga) melt may be utilized as the liquid electrode.

[0022] A method as defined by one further mode of the present invention, which employing the  $C/V$  technique profiles carrier concentration in a wafer including an In-containing-compound semiconductor surface layer, is characterized in contacting a metal Ga melt on the wafer surface, then solidifying the metal Ga melt to form a metal Ga electrode, employing an applied voltage that is up to a voltage surpassing 10V to

profile carrier concentration, and clearing away the metal Ga electrode after the profiling.

[0023] Another mode as defined by the present invention is characterized in that carrier concentration in a wafer including an In-containing-compound semiconductor surface layer is non-invasively profiled, and in that the wafer can be employed as it is, after its carrier concentration has been non-invasively profiled, for use in device processing. Here, this wafer may be one that has been profiled by any of the above-described non-invasive carrier-concentration profiling techniques.

[0024] In accordance with the present invention, carrier concentration/distribution within an In-containing compound semiconductor wafer may be non-invasively profiled to a depth of several  $\mu\text{m}$  in a short time and with a high degree of accuracy, and the profiled wafer itself may be provided for use directly in device fabrication.

[0025] From the following detailed description in conjunction with the accompanying drawings, the foregoing and other objects, features, aspects and advantages of the present invention will become readily apparent to those skilled in the art.

## Brief Description of Drawings

[0026] Fig. 1 is a graph plotting results of profiling, according to one mode of embodying the present invention, carrier concentration within a compound semiconductor wafer; and

[0027] Fig. 2 is a schematic block diagram representing one example of a conventional  $C/V$  analyzer.

## Detailed Description

[0028] Embodiment 1

[0029]

In a carrier concentration profiling method under a first embodiment, an improved electrochemical  $C/V$  technique is employed. A rebuilt version of the device in Fig. 2 may be utilized as the  $C/V$  analyzer for the improved electrochemical  $C/V$  technique. In particular, the electrical analyzing unit 6 was reformed to enable it to apply in excess of 10V and up to 60V as a reverse-bias applied voltage. Further, inasmuch as

photo-etching is unnecessary in the present invention, the light-receiving window 1b on the cell 1 is not required.

[0030] An aqueous solution of EDTA (ethylene diamine tetra-acetic acid) is utilized as an electrolyte 2'. The electrolyte 2' preferably contains 80 or more percent by mass EDTA. The reason why is because electrolysis of the water is thereby prevented when high voltage has been applied.

[0031] The carrier concentration/distribution in a compound semiconductor wafer utilized in fabricating optical communications devices was actually profiled in accordance with the present embodiment. The compound semiconductor wafer included, epitaxially grown in turn on an indium phosphate (InP) wafer: an InP layer of approximately  $1\ \mu\text{m}$  thickness, an indium-gallium arsenide (InGaAs) layer of approximately  $3\ \mu\text{m}$  thickness, and an InP layer of approximately  $2\ \mu\text{m}$  thickness. The epitaxial layers contained up to  $1 \times 10^{16}\ \text{cm}^{-3}$  dopant throughout. The Fig. 1 graph plots the results of profiling the carrier concentration/distribution in this compound semiconductor wafer. In the graph, from the surface of the wafer up to the depth of about  $1\ \mu\text{m}$  there is no curved line showing carrier concentration, because, there is a surface depletion layer through that depth.

[0032] In particular, the horizontal scale in the Fig. 1 graph indicates the depth  $w\ (\mu\text{m})$  from the surface of the epitaxial layers on, to the edge of the depletion layer in, the compound semiconductor wafer; while the vertical scale indicates the  $\log_{10}$  (common logarithm) of the carrier concentration  $N(\text{cm}^{-3})$  through the depth  $w$ . From this graph it may be confirmed that any one of the epitaxial layers had a carrier concentration of under  $1 \times 10^{16}\ \text{cm}^{-3}$ . It may likewise be confirmed that carrier concentration peaks are formed in positions corresponding to the locations of heterojunction interfaces that are at  $2\ \mu\text{m}$  and  $5\ \mu\text{m}$  from the wafer surface.

[0033] The profiling data in Fig. 1 was obtainable with an approximately 10-minute measurement. Furthermore, the Fig. 1 data is about the same as what would take 3 hours to profile while photo-etching using an aqueous HCl solution. On the other hand, inasmuch as photo-etching is not needed with the present invention, incidents of etching unevenness that require changing the measuring locale do not occur. What is more, profiling errors due to etching unevenness can be eliminated.



[0041] Embodiment 4

[0042] Embodiment 4 is similar to Embodiment 3 in that metal Ga is employed as an electrode. In Embodiment 4, however, a cell 1 like that illustrated in Fig. 2 is made unnecessary. In the carrier-concentration profiling method of Embodiment 4, to begin with a metal-Ga melt is soaked into a sponge-like retaining material. The retaining material is then contacted on the surface of a compound semiconductor wafer. Thus the wafer surface is wetted by and put in contact with the metal-Ga melt soaked into the sponge-like retaining material. The metal-Ga melt in this situation is then solidified, forming on the compound semiconductor wafer surface a solid metal-Ga electrode running along the sponge-like retaining material.

[0043] After utilizing the solid metal-Ga electrode to profile carrier concentration within the compound semiconductor wafer, the solid metal-Ga electrode is made molten once more to clear it from the wafer surface. The wafer from which the metal-Ga electrode has been cleared is itself then made available for device fabrication. In short, in terms of this embodiment as well, carrier concentration in a compound semiconductor wafer may be non-invasively profiled.

[0044] Only selected embodiments have been chosen to illustrate the present invention. To those skilled in the art, however, it will be apparent from the foregoing disclosure that various changes and modifications can be made herein without departing from the scope of the invention as defined in the appended claims. Furthermore, the foregoing description of the embodiments according to the present invention is provided for illustration only, and not for limiting the invention as defined by the appended claims and their equivalents.